IN THE DRAWINGS

Please replace Figures 1-7 with the amended version included herewith.

REMARKS

Claims 1-4 and 6-24 are pending in the application. Claim 5 is canceled.

The drawings are objected to for failure to show numerals discussed in the specification. Figures 3-7 are amended to include reference numerals and to correct an error in the depiction of metal stud 120. A replacement page is included to replace the original Figures 1-7 with the currently submitted Figures 1-7.

Claims 1, 3, 4, 9-11, 23 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 6,815,346 to Davis et al, hereinafter "Davis". Claims 1, 23 and 24 are independent. Applicants respectfully traverse this rejection.

Claim 1 provides a process for fabricating a low dielectric constant semiconductor. The process includes, *inter alia*, depositing a first metal layer on a substrate, patterning the first metal layer to form a patterned first metal wiring, and forming a support structure on the patterned first metal wiring using a stamp-contact printing technique. The support structure is a first insulating material having a dielectric constant K_1.

Davis discloses a process for fabricating copper-based semiconductor devices using low-k dielectric materials. A metal layer 52 makes contact to underlying semiconductor devices, such as transistors (col. 6, lines 7-9). A first level of copper metallization, which forms copper line 75, is reached from tungsten contact 52 through copper-filled via 77 (col. 6, lines 9-11). A low-k dielectric material layer 79 surrounds via 77, and may be applied by spin coating (col. 6, lines 12-14). This arrangement is then exposed and developed and an etch pattern is formed (col. 6, lines 20-22).

Davis discloses a process for manufacture of semiconductor devices using techniques including spin coating and etching. However, Davis does not disclose

forming a support structure **using a stamp contact printing technique**. Therefore, Davis does not disclose or suggest "forming a support structure on said patterned first metal wiring using a stamp contact printing technique, wherein said support structure is a first insulating material having a dielectric constant K_1," as recited in claim 1.

Thus, Davis fails to disclose or suggest the elements of claim 1. Therefore, claim 1 is patentable over Davis.

Claims 3, 4 and 9-11 depend from claim 1. For at least reasoning similar to that provided in support of the patentability of claim 1, claims 3, 4 and 9-11 are patentable over Davis.

Independent claims 23 and 24 include recitals similar to claim 1. For at least reasoning similar to that provided in support of the patentability of claim 1, claims 23 and 24 are patentable over Davis.

For the reasons set forth above, the rejection of claims 1, 3, 4, 9-11, 23 and 24 under 35 U.S.C. 102(b) as anticipated by Davis is overcome. Applicants respectfully request that the rejection of claims 1, 3, 4, 9-11, 23 and 24 be reconsidered and withdrawn.

Claims 1, 23 and 24 are also rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent Nos. 5,821,168 to Jain et al., 6,207,553 to Buynoski et al., 6,670,237 to Loh et al., and 6,815,329 to Babich et al., hereinafter collectively "the above references". Applicants respectfully traverse this rejection.

Claim 1 provides a process for fabricating a low dielectric constant semiconductor. The process includes, *inter alia*, depositing a first metal layer on a substrate, patterning the first metal layer to form a patterned first metal wiring, and forming a support structure on the patterned first metal wiring using a stamp-contact printing technique. The support structure is a first insulating material having a dielectric

constant K_1.

Applicants submit that none of the above references disclose or suggest forming a support structure **using a stamp contact printing technique**. Therefore, none of the above references disclose or suggest "forming a support structure on said patterned first metal wiring using a stamp contact printing technique, wherein said support structure is a first insulating material having a dielectric constant K_1," as recited in claim 1. Thus, the above references fail to disclose or suggest the elements of claim 1. Therefore, claim 1 is patentable over the above references.

Independent claims 23 and 24 include recitals similar to claim 1. For at least reasoning similar to that provided in support of the patentability of claim 1, claims 23 and 24 are patentable over the above references.

For the reasons set forth above, the rejection of claims 1, 23 and 24 under 35 U.S.C. 102(b) as anticipated by U.S. Patent Nos. 5,821,168 to Jain et al., 6,207,553 to Buynoski et al., 6,670,237 to Loh et al., and 6,815,329 to Babich et al., is overcome. Applicants respectfully request that the rejection of claims 1, 23 and 24 be reconsidered and withdrawn.

Claims 2, 5-8, 12-13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis. Claim 5 is canceled. Claims 2, 5-8, 12-13 and 15-16 depend from claim 1. Applicants respectfully traverses this rejection.

As discussed above, Davis does not disclose or suggest "forming a support structure on said patterned first metal wiring using **a stamp contact printing technique**, wherein said support structure is a first insulating material having a dielectric constant K_1," as recited in claim 1.

The Office Action states that it is well known in the art that insulating material can be formed by contact printing. Applicants respectfully disagree and submit that those

skilled in the art would not consider using a contact printing technique to form supporting structures on a semiconductor. Therefore, Applicants submit that there is no motivation to combine the teachings of Davis with knowledge in the art of contact printing.

Contact printing is known in the art, however it is not generally known to be applied in manufacturing semiconductor devices such as semiconductor chips and other high-end circuitry. Contact printing presents difficulties in precisely aligning desired patterns, and also presents difficulties in potentially damaging a substrate because of contact between, e.g., a stamp and the substrate. Therefore, more precise non-contact techniques such as microlithography are preferred for semiconductor applications. Thus, although contact printing is utilized for low precision applications such as thin film display, it is not generally desirable for manufacturing semiconductor wafers and other devices that require a highly precise alignment of features.

Davis, which describes methods for manufacturing a multi-layer semiconductor device, would not benefit from simply using a contact printing method as described above. Indeed, as discussed above, the knowledge in the art would suggest to one skilled in the art that contact printing would be unsuitable for use in methods such as described in Davis.

Thus, there is no suggestion or motivation to combine Davis with the knowledge cited by the Office Action. Therefore, claims 2, 6-8, 12-13 and 15-16 are patentable over the combination cited by the Office Action. Applicants respectfully request that the section 103 rejection of claims 2, 5-8, 12-13 and 15-16 be reconsidered and withdrawn.

Claims 14 and 17-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Davis in view of U.S. Patent No. 6,815,346 to Babich et al., hereinafter "Babich". Claims 14 and 17-22 depend from claim 1. Applicants respectfully traverses this rejection.

As discussed above, Davis does not disclose or suggest "forming a support structure on said patterned first metal wiring using **a stamp contact printing technique**, wherein said support structure is a first insulating material having a dielectric constant K_1," as recited in claim 1. Therefore, claim 1 is patentable over Davis. Applicants do not believe that Babich makes up for the deficiencies of Davis, as they apply to claim 1. Thus, claim 1 is patentable over the cited combination of Davis and Babich.

Claims 14 and 17-21 depend from claim 1. For at least reasoning similar to that provided in support of the patentability of claim 1, claims 14 and 17-21 are patentable over the cited combination of Davis and Babich.

For the reasons set forth above, the rejection of claims 14 and 17-21 under 35 U.S.C. 102(b) as unpatentable over Davis in view of Babich is overcome. Applicants respectfully request that the rejection of claims 14 and 17-21 be reconsidered and withdrawn.

An indication of the allowability of all pending claims by issuance of a Notice of Allowability is earnestly solicited.

Respectfully submitted,

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